UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,141	02/03/2004	Heon Lee	4366-040241	1895

28289 7590 09/20/2005

THE WEBB LAW FIRM, P.C.
700 KOPPERS BUILDING
436 SEVENTH AVENUE
PITTSBURGH, PA 15219

EXAMINER	
BUDD, PAUL A	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,141	LEE, HEON	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~3 Feb 2005~~. 9/20/4
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 14-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on July 5,2005.

Specification

2. The disclosure is objected to because of the following informalities: the specification contains several typographical and/or grammatical errors. For example:

Page 6, line 10, change "complicate" to "complicated",

Page 15, line 1, change "replaced" with "replace",

Page 16, line 8, change "are there" to "there are",

Page 16, line 12, change "cover" to "covers"

Page 18, line 19, change "737" at the beginning of the sentence to "735",

Page 21, line 17, change "seems" to "seams"

Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 610 in Figure 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet

should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 17,18,19,23,24,25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for the device claims 18,23,24,25, it is not possible to tell the difference between a hole in the thin dielectric referred to as a "damaged spot" as opposed to a "pore". As for the limitation "damaged spot", it is unclear what the structure would look like .For the purposes of this Office Action the term "pore" and "damaged spot" will be treated as referring to the same structure.

The phrase "large lithographic margin " in claims 17,19 is a relative term, which renders the claims indefinite. The term “large lithographic margin” is indefinite and draws a comparison to an unknown. The specification does not define normal lithographic margin.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 16,18 (as best understood) are rejected under 35 U.S.C. 102 (b) as being anticipated by Wolstenholme el al (US Patent 5,751,012).

Regarding claims 16,18,

Wolstenholme teaches, a phase-change memory device [Fig. 2 or Fig.3, 330] comprising:

(a) a lower dielectric layer [Fig. 3, 34];

(b) a lower electrode [26], at least a part of the lateral surface of the lower electrode [26] being surrounded by the lower dielectric layer [Fig. 3, 34];

(c) a thin dielectric layer [Fig. 3, 28] including a pore (“damaged spot”) having smaller area than the top surface of the lower electrode [26], aligned to the top surface of the lower electrode [26] and extending to the top surface of the lower electrode [26]; and

(d) a phase-change resistor [30, 28a] filling the pore (“damaged spot”) and formed on the thin dielectric layer [Fig. 3, 28].

6. Claims 16,18 (as best understood) are rejected under 35 U.S.C. 102 (b) as being anticipated by Wolstenholme el al (US Patent 6,236,059).

Regarding claims 16,18,

Wolstenholme teaches, a phase-change memory device [Fig. 6, 75] comprising:

(a) a lower dielectric layer [Fig. 6, 80];

(b) a lower electrode [22], at least a part of the lateral surface of the lower electrode [22] being surrounded by the lower dielectric layer [80];

(c) a thin dielectric layer [45] including a pore ("damaged spot") [50] having smaller area than the top surface of the lower electrode [22], aligned to the top surface of the lower electrode [22] and extending to the top surface of the lower electrode [22]; and

(d) a phase-change resistor [55] filling the pore ("damaged spot") [50] and formed on the thin dielectric layer [45].

7. Claims 16,18 (as best understood) are rejected under 35 U.S.C. 102 (b) as being anticipated by Maimon (US Patent Pub. 2002/0197566).

Regarding claims 16,18,

Maimon et al teaches, a phase-change memory device [Fig. 16] comprising:

(a) a lower dielectric layer [Fig. 16, 110];

(b) a lower electrode [134], at least a part of the lateral surface of the lower electrode [134] being surrounded by the lower dielectric layer [110];

(c) a thin dielectric layer [150] including a pore ("damaged spot") [200] having smaller area than the top surface of the lower electrode [134], aligned to the top surface of the lower electrode [134] and extending to the top surface [202] of the lower electrode [134]; and

(d) a phase-change resistor [210] filling the pore ("damaged spot") [200] and formed on the thin dielectric layer [150].

8. Claims 16,18 (as best understood) are rejected under 35 U.S.C. 102 (b) as being anticipated by Klersy et al (US Patent 5,536,947).

Regarding claims 16,18,

Klersy et al teaches, a phase-change memory device [Fig. 1, 30] comprising:

(a) a lower dielectric layer [Fig. 1, 39];

(b) a lower electrode [32, 34], at least a part of the lateral surface of the lower electrode [32, 34] being surrounded by the lower dielectric layer [39];

(c) a thin dielectric layer [46, 48] including a pore ("damaged spot") [Column 17, lines 20-67 and column 18, lines 1-18, discusses pore/damaged-spot formation. Particularly, "The filament confining means plays a role in the 'electrical formation process' of the memory device. The electrical formation process consists of applying higher current electrical pulses to the newly constructed memory element until the memory element switches from its originally very high 'virgin' resistance value to a lower resistance value. Once this occurs, the memory element is said to be 'formed'. It is now ready for

subsequent lower current electrical cycling."] having smaller area than the top surface of the lower electrode [32, 34], aligned to the top surface of the lower electrode [32, 34] and extending to the top surface of the lower electrode [32, 34]; and

(d) a phase-change resistor [36] filling the pore ("damaged spot") and formed on the thin dielectric layer [46, 48].

9. Claims 20,21,22,23,24,25 (as best understood), are rejected under 35 U.S.C. 102 (b) as being anticipated by Zahorik el al (US Patent Pub. 2002/0006735).

Regarding claims 20,23,

Zahorik teaches, a phase-change memory device [Fig. 4, 18] comprising:

(a) a lower dielectric layer [52];

(b) a lower phase-change resistor [28], at least a part of the lateral surface of the lower phase-change resistor [28] being surrounded by the lower dielectric layer [52]; and

(c) a thin dielectric layer [36] including a pore ("damaged spot") having smaller area than the top surface of the lower phase-change resistor [28], aligned to the top surface of the lower phase-change resistor [28] and extending to the top surface of the lower phase-change resistor [28].

Regarding claims 21,24,

Zahorik teaches, the phase-change memory device [Fig. 4, 18] as set forth in claim 20 (or claim 23), further comprising:

(d) an upper electrode [Fig. 4, 32] filling the pore ("damaged spot") and formed on the thin dielectric layer [36].

Regarding claims 22,25, Zahorik teaches,

The phase-change memory device [Fig. 4, 18] as set forth in claim 20 (or claim 23), further comprising:

(d) an upper phase-change resistor [the space marked by 34] filling the pore and formed on the thin dielectric layer [36].

The claim does not differentiate between material differences between the phase change material below the pore and the material filling the pore.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 20,21,23,24 (as best understood) are rejected under 35 U.S.C. 102 (e) as being anticipated by Horii el al (US Patent Pub. 2003/0209746).

Regarding claims 20,23,

Horii teaches, a phase-change memory device [Fig. 2A] comprising:

(a) a lower dielectric layer [Fig. 2A, 75, 66];

(b) a lower phase-change resistor [Fig. 2A; 69,71; Page 4 paragraph 0031,"The oxidation resistant layer, the phase change material and the first barrier layer are successively patterned to form a plurality of data storage elements... Each of the data storage elements is composed of a first barrier pattern 69 and a phase change material layer pattern 71 stacked on the first barrier layer pattern 69."], at least a part of the lateral surface of the lower phase-change resistor [69,71] being surrounded by the lower dielectric layer [75]; and

(c) a thin dielectric layer [Fig. 6, 79; Page 4 paragraph 0033, "The insulating spacers 79 may be formed of a silicon oxide layer or a silicon nitride layer."] including a pore ("damaged spot") having smaller area than the top surface of the lower phase-change resistor [69,71], aligned to the top surface of the lower phase-change resistor [69,71] and extending to the top surface of the lower phase-change resistor [69,71].

Regarding claims 21,24,

Horii teaches, the phase-change memory device [Fig. 2A] as set forth in claim 20 (or claim 23), further comprising:

(d) an upper electrode [Fig. 2A; 81,83] filling the pore ("damaged spot") and formed on the thin dielectric layer [Fig. 2A, 79].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 17,19, (as best understood) are rejected under 35 U.S.C. 103(a) as being unpatentable over Klersy et al in view of Sadjadi et al (US Pat. 6,495,470).

Klersy teaches,

a phase-change memory device [Fig. 1, 30] comprising:

(a) a lower dielectric layer [Fig. 1, 39];

(b) a lower electrode [32, 34], at least a part of the lateral surface of the lower electrode [32, 34] being surrounded by the lower dielectric layer [39];

(c) a thin dielectric layer [46, 48] including a pore ("damaged spot") [Column 17, lines 20-67 and column 18, lines 1-18, discusses pore/damaged-spot formation. Particularly, "The filament confining means plays a role in the 'electrical formation process' of the memory device. The electrical formation process consists of applying higher current electrical pulses to the newly constructed memory element until the memory element switches from its originally very high 'virgin' resistance value to a lower resistance value. Once this occurs, the memory element is said to be 'formed'. It is now ready for subsequent lower current electrical cycling."] having smaller area than the top

surface of the lower electrode [32, 34], aligned to the top surface of the lower electrode [32, 34] and extending to the top surface of the lower electrode [32, 34]; and

(d) a phase-change resistor [36] filling the pore ("damaged spot") and formed on the thin dielectric layer [46, 48].

However Klersy fails to teach, "wherein the lower electrode is filling a recessed part having a tapered sidewall in the lower dielectric layer so that the top surface area of the lower electrode is larger than the bottom surface area;

and wherein large lithographic margin is provided owing to the large top surface area." However, Sadjadi et al teaches a tapered via. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sadjadi into Klersy. The ordinary artisan would have been motivated to modify Klersy for the purpose of "the tapered profile of via opening 306 is easier to fill than a vertical via." [Column 8, lines 52-54].

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, see reference Broklin et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number is 571-272-1664. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER